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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PHUNG, ANH K

ART UNIT PAPER NUMBER

2824

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/680,483

Applicant(s)

TRAN ET AL

Examiner

ANH PHUNG

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 June 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6, 13, 15-18, 20 and 25 is/are rejected.
- 7) ☒ Claim(s) 7-12, 14, 19, 21-24 and 26 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Detailed Action

1. This Office Action is responsive to the Election received on June 6, 2005, claims **26-30** are cancelled and claims **1-26** are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **1-6, 13, 15-18, 20** and **25** are rejected under 35 U.S.C. 102(e) as being anticipated by Iwata et al. (U.S. Pat. No. 6,795,334).

Regarding independent claim **1**, Iwata et al disclose a data storage device comprising a cross point array of resistive memory elements (12, Fig. 4) and a plurality of blocking elements (diode DI, Fig. 4), the memory elements and the blocking elements arranged in groups (BK0n-Bk00 & BKjn-BKj0, Fig. 4), each group including series-connected memory elements (12, Fig. 4), and a blocking element (diode DI, Fig. 4).

Regarding dependent claim **2**, Iwata et al disclose the memory elements include magnetoresistive elements (magnetoresistive effect in claim 1, col. 87).

Regarding dependent claim **3**, Iwata et al disclose the memory elements include tunneling magnetoresistive elements (a tunneling barrier layer in claim 24, col. 89).

Regarding dependent claim **4**, Iwata et al disclose the blocking elements include diodes (Fig. 4, diode DI).

Regarding dependent claim **5**, Iwata et al disclose the blocking elements include transistors (transistors RSW, Fig. 4).

Regarding dependent claim **6**, Iwata et al further disclose a substrate (41, Fig. 2), the blocking elements (RSW, Fig. 2) formed on the substrate.

Regarding dependent claim **13**, Iwata et al disclose a circuit for performing destructive read operations on the memory elements (lines 30-39, col. 29).

Regarding independent claim **15**, Iwata et al disclose an MRAM device comprising a cross point array of tunneling magnetoresistive memory elements (12, Fig. 4); and a plurality of sneak path blocking elements (diode DI, Fig. 4); the device arranged in groups, each group including at least two memory elements (BK0n, Fig. 4) and at least one blocking device (diode DI, Fig. 4) connected in series.

Regarding dependent claim **16**, Iwata et al disclose wherein the blocking elements include diodes (diode DI, Fig. 4).

Regarding dependent claim **17**, Iwata et al disclose wherein the blocking elements include transistors (transistors RSW, Fig. 4).

Regarding dependent claim **18**, Iwata et al disclose, further comprising a substrate (41, Fig. 2), the array and the blocking elements (RSW, Fig. 2) formed on the substrate.

Regarding dependent claim **20**, Iwata et al disclose, further comprising a plurality of first and second read lines (BL0-BLj & RWL0-RWLn, Fig. 4), the first read lines being

Art Unit: 2824

orthogonal to the second read lines, each group connected between one of the first read lines and one of the second read lines.

Regarding dependent claim **25**, Iwata et al disclose, further comprising a circuit for performing destructive read operations on the memory elements (lines 30-39, col. 29).

Allowable Subject Matter

4. Claims **7-12, 14** and **19, 21-24, 26** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is no teaching:

“wherein each group includes a discontinuous conductor for connecting the memory elements and the blocking element in series” as claimed in the dependent claims **7-12**; or

“a circuit for determining a logic value stored in a selected memory element of a selected group, the circuit causing a sense current to flow through the selected group, sampling the sense current and storing the sampled value, writing a logic value to the selected memory element in the selected group, causing a sense current to flow through the selected group, and sampling the sense current and comparing the second sampled value to the stored value” as claimed in the dependent claim **14**; or

“each group includes a discontinuous conductor for connecting the memory elements and the blocking element in series” as claimed in the dependent claim **19**; or

“a circuit for applying a first potential to a selected first read line, and a second potential to a selected second read line during a read operation on a selected memory

Art Unit: 2824

element, a difference between the first and second potentials causing a sense current to flow through a group including the selected memory element” as claimed in the dependent claims **21-24**; or

“comprising a circuit for determining a logic value stored in a selected memory element of a selected group, the circuit causing a sense current to flow through the selected group, sampling the sense current and storing the sampled value, writing a logic value to the selected memory element in the selected group, causing a sense current to flow through the selected group, and sampling the sense current and comparing the second sampled value to the stored value” as claimed in the dependent claim **26**.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ezaki et al. (US 2004/0114425) and Eaton, Jr. et al. (US 2005/0094458) disclose an MRAM memory similar to that of Iwata et al. (US 6,795,334).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **ANH PHUNG** whose telephone number is **(571) 272-1883**. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **RICHARD ELMS**, can be reached on **(571) 272-1869**. The fax phone

Art Unit: 2824

number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **866-217-9197** (toll-free).

Art Unit: 2824

AKP

A handwritten signature in black ink, appearing to read 'Anh Phung', written in a cursive style.

**ANH PHUNG
PRIMARY EXAMINER**